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User's Manual

Renesas Starter Kit for H8/36079

User's Manual

RENESAS SINGLE-CHIP MICROCOMPUTER
H8 FAMILY/ H8/300H Tiny Series

Renesas Electronics
www.renesas.com

Rev.1.00 2007.10

Table of Contents

Chapter 1. Preface

Cautions

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Glossary

CPU	Central Processing Unit	RTE	Renesas Technology Europe Ltd.
HEW	High-performance Embedded Workshop	RSO	Renesas Solutions Organisation.
LED	Light Emitting Diode	RSK	Renesas Starter Kit
PC	Program Counter	E8A	E8A On-chip debugger module

Chapter 2.Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as Switches, LEDs and potentiometer.
- User or Example Application.
- Sample peripheral device initialisation code.

The RSK board contains all the circuitry required for microcontroller operation.

Chapter 3.Power Supply

3.1. Requirements

This RSK operates from a 5V power supply.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All RSK boards are supplied with an E8A debugger. This product is able to power the RSK board with up to 300mA. When the RSK is connected to another system then that system should supply power to the RSK.

All RSK boards have an optional centre positive supply connector using a 2.0mm barrel power jack.

Warning

The RSK is neither under nor over voltage protected. Use a centre positive supply for this board.

3.2. Power – Up Behaviour

When the RSK is purchased the RSK board has the ‘Release’ or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. After 200 flashes, or after pressing a switch the LEDs will flash at a rate controlled by the potentiometer.

Chapter 4. Board Layout

4.1. Component Layout

The following diagram shows top layer component layout of the board.

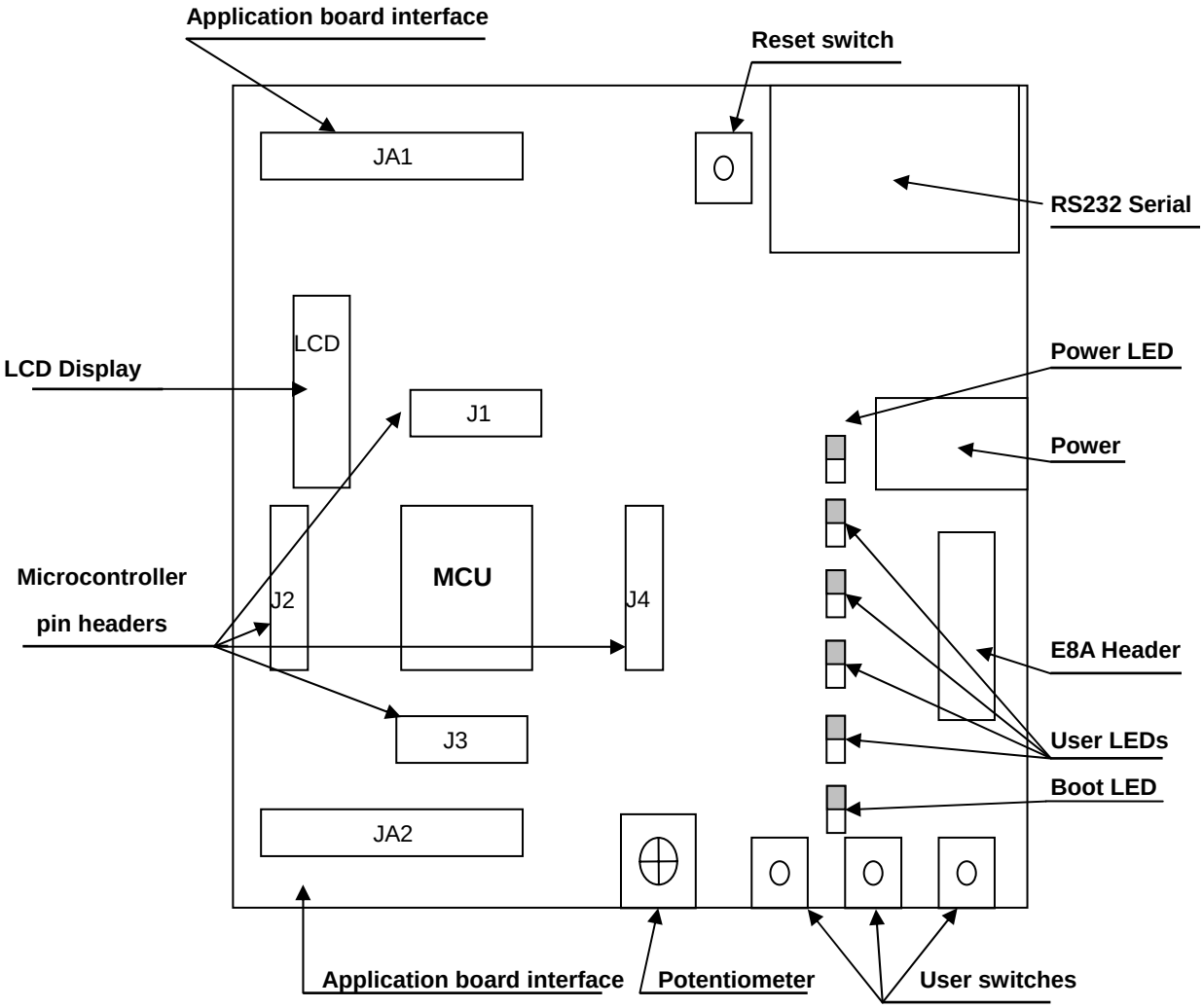

Figure 4-1: Board Layout

4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

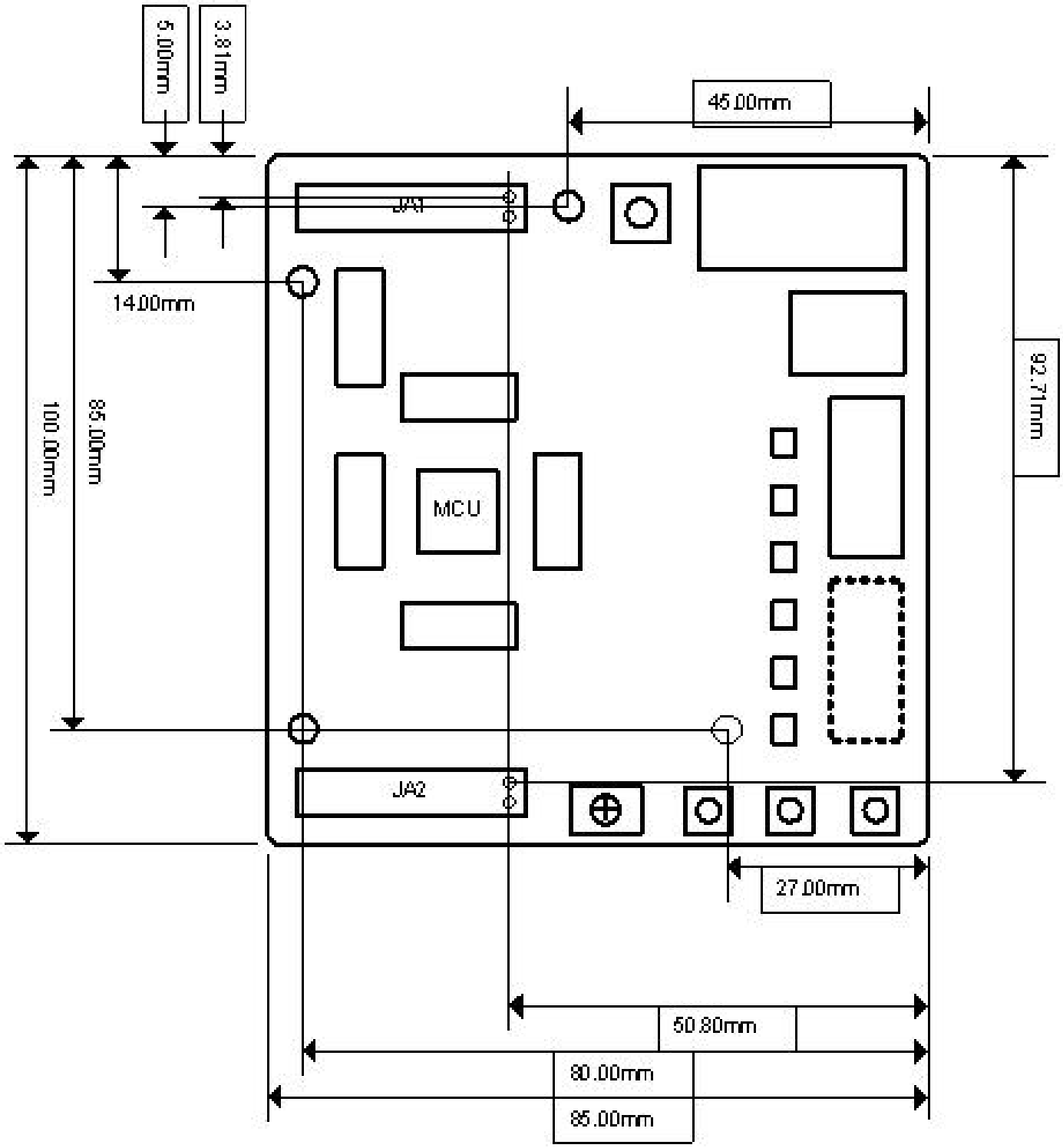

Figure 4-2 : Board Dimensions

Chapter 5. Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.

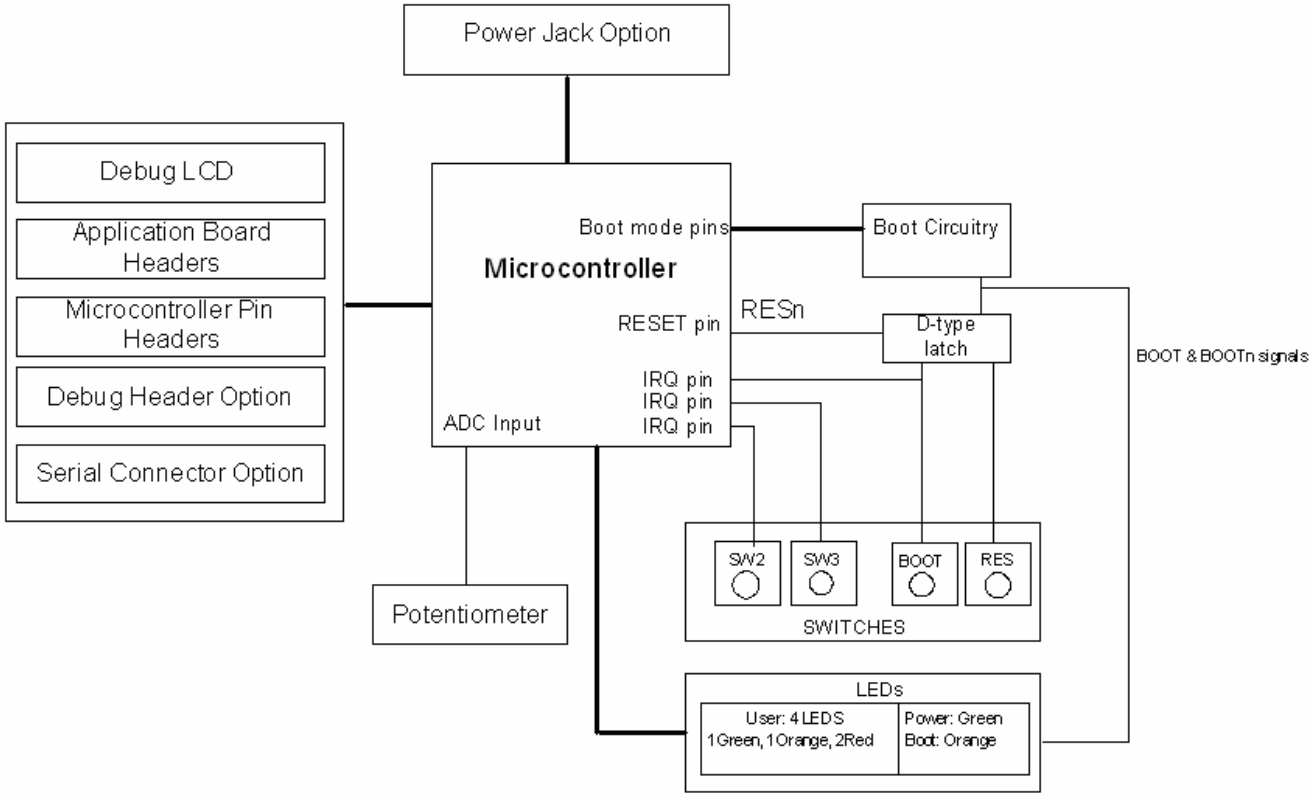

Figure 5-1: Block Diagram

Figure 5-2 shows the connections to the RSK.

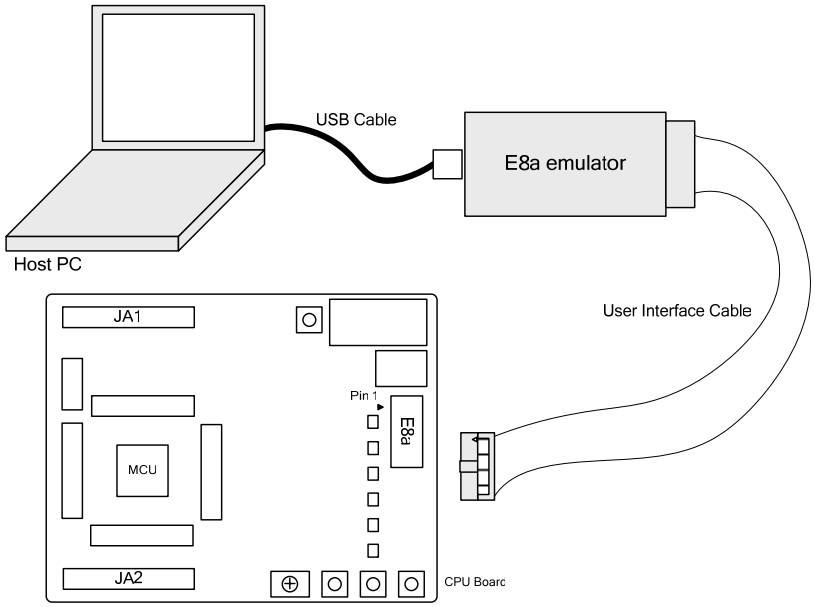

Figure 5-2 : RSK Connections

Chapter 6. User Circuitry

6.1. Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in Table 6-1.

Switch	Function	Microcontroller
RES	When pressed, the RSK microcontroller is reset.	RESn, Pin7
SW1/BOOT*	Connects to an IRQ input for user controls. The switch is also used in conjunction with the RES switch to place the device in BOOT mode when not using the E8A debugger.	WKP5/ADTRG, Pin 22 (Port 5 pin 5)
SW2*	Connects to an IRQ line for user controls.	IRQ2n, Pin 53 (Port 1, pin 6)
SW3*	Connects to the ADC trigger input. Option link allows connection to IRQ line. The option is a pair of 0R links. For more details on option links, please refer to Sec 6.6.	IRQ0n, Pin 51 (Port 1, pin 4)

Table 6-1: Switch Functions

*Refer to schematic for detailed connectivity information.

6.2. LEDs

There are six LEDs on the RSK board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in BOOT mode when lit. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low.

Table 6-2, below, shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Colour	Microcontroller Port Pin function	Microcontroller Pin Number
LED0	Green	Port 5.4	21
LED1	Orange	Port 1.0	23
LED2	Red	Port 2.3	47
LED3	Red	Port 1.7	54

Table 6-2: LED Port

6.3. Potentiometer

A single turn potentiometer is connected to AN4 (PB.4) of the microcontroller. This may be used to vary the input analogue voltage value to this pin between AVCC and Ground.

6.4. Serial port

Serial port SCI3 is connected to the standard RS232 header. Serial port SCI3_2 can optionally be connected to the RS232. The connections to be fitted are listed in the table 6-3.

Description	Function	Circuit Net Name	Device Pin
SCI3	Programming serial port	TxD	46
SCI3	Programming serial port	RxD	45
SCI3_2	Spare Serial Port	TxD2	50
SCI3_2	Spare Serial Port	RxD2	49

Table 6-3: Serial Port settings

The SCI3_2 port is also available on J4 and JA2. The SCI3 port is available on J3.

6.5. Debug LCD Module

A debug LCD module is supplied to be connected to the connector LCD. This should be fitted so that the debug LCD module lies over J1. Care should be taken to ensure the pins are inserted correctly into LCD. The debug LCD module uses a 4 bit interface to reduce the pin allocation. No contrast control is provided; this is set by a resistor on the supplied display module. The module supplied with the RSK only supports 5V operation.

Table 6-4 shows the pin allocation and signal names used on this connector.

LCD					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Ground	-	2	5V Only	-
3	No Connection	-	4	DLCDRS (P24)	31
5	R/W (Wired to Write only)	-	6	DLCDE+ 100k pull down to ground (P12)	25
7	No Connection	-	8	No connection	-
9	No Connection	-	10	No connection	-
11	DLCDD4 (P50)	13	12	DLCDD5 (P51)	14
13	DLCDD6 (P52)	19	14	DLCDD7 (P53)	20

Table 6-4 Debug LCD Module Connections

6.6. Option Links

Table 6-5 below describes the function of the option links associated with E8A configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R2	E8A	Fitted if one of the following condition is satisfied: 1. The CPU operating voltage is 5V 2. E8A is used to supply 3V3 to the board	Removed if none of the conditions are satisfied	R5, R7, R9, R10
R5	E8A	Fitted if one of the following condition is satisfied: 1. The CPU operating voltage is 5V 2. E8A is used to supply 3V3 to the board	Removed if none of the conditions are satisfied	R2, R7, R9, R10
R7	E8A	Fitted if one of the following condition is satisfied: 1. The CPU operating voltage is 5V 2. E8A is used to supply 3V3 to the board	Removed if none of the conditions are satisfied	R2, R5, R9, R10
R9	E8A	Fitted if one of the following condition is satisfied: 1. The CPU operating voltage is 5V 2. E8A is used to supply 3V3 to the board	Removed if none of the conditions are satisfied	R2, R5, R7, R10
R10	E8A	Fitted if one of the following condition is satisfied: 1. The CPU operating voltage is 5V 2. E8A is used to supply 3V3 to the board	Removed if none of the conditions are satisfied	R2, R5, R7, R9
R11	E8A	Enables E8A		

Table 6-5: E8A configuration links

Table 6-6 below describes the function of the option links associated with Serial Port configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R16	Serial Port Configuration	Connects serial port SCI3_2 (Rx) to D-type connector (SERIAL).	**Disconnects serial port SCI3_2 (Tx) from D-type connector (SERIAL).**	R18
R18	Serial Port Configuration	Connects serial port SCI3_2 (Tx) to D-type connector (SERIAL).	**Disconnects serial port SCI3_2 (Rx) from D-type connector (SERIAL).**	R16
R40	Serial Port Configuration	Disables Serial Communication	**Enables Serial Communication**	

Table 6-6: Serial Port configuration links

Table 6-7 below describes the function of the option links associated with Power Source configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R20	Power Source	**Board can be powered from PWR connector**	Disable external power connector	
R28	Power Source	**Fitted if CPU operating voltage is 3V3**	Removed if CPU operating voltage is not 3V3	R29, R30
R29	Power Source	Fitted if CPU operating voltage is 5V	**Removed if CPU operating voltage is not 5V**	R28, R30
R30	Power Source	**Board can be powered from external source (JA1 header pin 1)**	Board can't be powered from external source (JA1 header pin 1)	R28, R29
R31	Power Source	Fitted if CPU operating voltage is 3V3	**Removed if CPU operating voltage isn't 3V3**	R32
R32	Power Source	**Fitted if CPU operating voltage is 5V**	Removed if CPU operating voltage is not 5V	R31
R33	Power Source	**Enables Low Voltage Detection (LVD) Circuitry.**	Disables Low Voltage Detection (LVD) Circuitry. Can be enables jumper J6 set	
R47	Power Source	Board can be powered from external source (JA1 header pin 2)	**Board can't be powered from external source (JA1 header pin 2)**	
R54	Power Source	Fitted if 3V3 device	**Removed if not 3V3 device**	

Table 6-7: Power configuration links

Table 6-8 below describes the function of the option links associated with CPU Reset configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R38	CPU reset signal	**Enables CPU reset signal**	Disables CPU reset signal, but it can be enabled if jumper J7 set	

Table 6-8: Reset configuration links

Table 6-9 below describes the function of the option links associated with Analog Voltage Source configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R42	Analog Voltage Source	Analog Voltage Source from external connector. (JA1 header pin 1)	**Analog voltage source from on board Vcc.**	R43
R43	Analog Voltage Source	**Analog voltage source from on board Vcc.**	Analog Voltage Source from external connector.	R42

Table 6-9: Analog Voltage Source configuration links

Table 6-10 below describes the function of the option links associated with External Subclock Oscillator configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R49	External Subclock Oscillator	Parallel resistor for crystal	**Not fitted**	

Table 6-10: External Subclock Oscillator configuration links

Table 6-11 below describes the function of the option links associated with Real Time Clock Oscillator Source configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R50	Real Time Clock Oscillator Source	External Clock Source	**Internal Clock Source**	R49, R52, R53
R52	Real Time Clock Oscillator Source	**Internal Clock Source**	External Clock Source	R49, R50, R53
R53	Real Time Clock Oscillator Source	External Clock Source	**Internal Clock Source**	R49, R50, R52

Table 6-11: Real Time Clock Oscillator Source configuration links

Table 6-12 below describes the function of the option links associated with Processor Oscillator Source configuration. The default configuration is indicated by **BOLD** text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R56	Processor Oscillator Source	External Clock Source	**Internal Clock Source**	R59, R60, R61, R64
R59	Processor Oscillator Source	**Internal Clock Source**	External Clock Source	R56, R60, R61, R64
R61	Processor Oscillator Source	**Internal Clock Source**	External Clock Source	R56, R59, R60, R64
R64	External main Oscillator	**External Clock Source**	Internal Clock Source	R59, R60, R61 R56

Table 6-12: Processor Oscillator Source configuration links

Table 6-13 below describes the function of the option links associated with other configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R57	ADTRGn	Enables ADTRGn signal	**Disables ADTRGn signal**	R58
R58	WKP	**Enables WKP signal**	Disables WKP signal	R57

Table 6-13: Other configuration links

Table 6-14 below describes the function of the option links associated with External main Oscillator configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R60	External main Oscillator	Parallel resistor for crystal	**Not fitted**	

Table 6-14: External main Oscillator configuration links

Table 6-15 below describes the function of the option links associated with IIC configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R66	IIC Data	**Enables IIC data transmission**	Disables IIC data transmission	R68
R68	IIC Clock	**Enables IIC clock**	Disables IIC clock	R66

Table 6-15: IIC configuration links

6.7. Oscillator Sources

A crystal oscillator is fitted on the RSK and used to supply the main clock input to the Renesas microcontroller. Table 6-6 details the

oscillators that are fitted and alternative footprints provided on this RSK:

Component		
Crystal (X1)	Fitted	32.768 KHz (90SMX package)
Crystal (X2)	Fitted	20 MHz (HC49/4H package)

Table 6-6: Oscillators / Resonators

6.8. Reset Circuit

The CPU Board includes a simple latch circuit that links the mode selection and reset circuit. This provides an easy method for swapping the device between Boot Mode and User mode. This circuit is not required on customer's boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK. Please refer to the hardware manual for more information on the requirements of the reset circuit.

The Reset circuit operates by latching the state of the boot switch on pressing the reset button. This control is subsequently used to modify the port pin P24 states as required.

The port pin P24 must change state only while the reset signal is active to avoid possible device damage.

The reset is held in the active state for a fixed period by a pair of resistors and a capacitor. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7. Modes

This RSK supports Boot mode and User mode.

Details of programming the FLASH memory is described in the H8/38347 Group Hardware Manual.

7.1. Boot mode

The boot mode settings for this RSK are shown in Table 7-1: Boot Mode pin settings below:

TEST	NMI	P85	LSI State after Reset End
0	Low	High	Boot Mode

Table 7-1: Boot Mode pin settings

The software supplied with this RSK supports Boot mode using an E8A and HEW only. However, hardware exists to enter boot mode manually, do not connect the E8A in this case. Press and hold the SW1/BOOT. The pin NMI (microcontroller pin 35) is held in its boot state while reset is pressed and released. Release the boot button. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.

When neither the E8A is connected nor the board is placed in boot mode as above, the TEST pin is connected to Ground; the NMI pin is pulled high by a 10k resistor, the P8.5 pin is pulled high with a 4.7k resistor.

When an E8A is used the port P85 and NMI are controlled by the E8A.

7.2. User mode

Because the NMI pin is pulled high, this RSK will always boot in User mode when the E8A is not connected and the boot switch is not depressed. Refer to H8/36079 Group Hardware Manual for details of User mode. The user mode settings for this RSK are shown in Table 7-1: Boot Mode pin settings below:

TEST	NMI	P85	LSI State after Reset End
0	High	X	User Mode

X: Don't care

Table 7-2: User Mode pin settings

Chapter 8. Programming Methods

The board is intended for use with HEW and the supplied E8A debugger. Refer to H8/36079 Group Hardware Manual for details of programming the microcontroller without using these tools.

Chapter 9. Headers

9.1. Microcontroller Headers

Table 9-1 to Table 9-4 show the microcontroller pin headers and their corresponding microcontroller connections. The header pins connect directly to the microcontroller pin unless otherwise stated.

J1					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	PIN1	1	2	PIN2	2
3	AVCC	3	4	CON_X2	4
5	CON_X1	5	6	NC	6
7	RESn	7	8	NC	8
9	Ground	9	10	CON_OSC2	10
11	CON_OSC1	11	12	UC_VCC	12
13	DLCDD4	13	14	DLCDD5	14
15	IO_4	15	16	IO_5	16

Table 9-1: J1

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	IO_6	17	2	IO_7	18
3	DLCDD6	19	4	DLCDD7	20
5	LED0	21	6	WKP_ADTRGn	22
7	LED1	23	8	TRISTn	24
9	DLCDE	25	10	PIN26	26
11	PIN27	27	12	TRIGa	28
13	TRIGb	29	14	TMR0	30
15	DLCDRS	31	16	Un	32

Table 9-2: J2

J3					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	TMR1	33	2	Up	34
3	NMIn	35	4	UD	36
5	Vp	37	6	Wp	38
7	Vn	39	8	Wn	40
9	PTRX	41	10	PTTX	42
11	PTCK	43	12	SCK3	44
13	RXD	45	14	TXD	46
15	LED2	47	16	SCK3_2	48

Table 9-3: J3

J4					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	RXD_2	49	2	TXD_2	50
3	IRQ0n	51	4	IRQ1n	52
5	IRQ2n	53	6	LED3	54
7	IO_3	55	8	IO_2	56
9	IO_1	57	10	IO_0	58
11	AN3	59	12	AN2	60
13	AN1	61	14	AN0	62
15	AD_POT	63	16	PIN64	64

Table 9-4: J4

9.2. Application Headers

Table 9-5 and Table 9-6 below show the standard application header connections.

JA1							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	5V	CON_5V	-	2	0V	GROUND	-
3	3V3	CON_3V3	-	4	0V	GROUND	-
5	AVCC	CON_AVCC	3	6	AVss	NC	-
7	AVref	CON_AVREF	-	8	ADTRG	ADTRGn	22
9	AD0	AN0	62	10	AD1	AN1	61
11	AD2	AN2	60	12	AD3	AN3	59
13	DAC0	NC	-	14	DAC1	NC	-
15	IO_0	IO_0	58	16	IO_1	IO_1	57
17	IO_2	IO_2	56	18	IO_3	IO_3	55
19	IO_4	IO_4	15	20	IO_5	IO_5	16
21	IO_6	IO_6	17	22	IO_7	IO_7	18
23	IRQ3	WKP	22	24	IIC_EX	NC	-
25	IIC_SDA	SDA	26	26	SCL	SCL	27

Table 9-5: JA1 Standard Generic Header

JA2							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	RESn	RESn	7	2	EXTAL	CON_OSC1	11
3	NMIn	NMIn	35	4	VSS1	GROUND	-
5	WDT_OVF	-	-	6	SCIaTX	TXD2	50
7	IRQ0	IRQ0	51	8	SCIaRX	RXD2	49
9	IRQ1	IRQ1	52	10	SCIaCK	SCK3_2	48
11	UD	UD	36	12	CTS/RTS	NC	-
13	Up	Up	34	14	Un	Un	32
15	Vp	Vp	37	16	Vn	Vn	39
17	Wp	Wp	38	18	Wn	Wn	40
19	TMR0	TMR0	30	20	TMR1	TMR1	33
21	TRIGa	TRIGa	28	22	TRIGb	TRIGb	29
23	IRQ2	IRQ2n	53	24	TRISTn	TRISTn	24
25	-	-		26	-	-	-

Table 9-6: JA2 Standard Generic Header

Chapter 10.Code Development

10.1. Overview

Note: For all code debugging using Renesas software tools, the RSK board must be connected to a PC USB port via an E8A. An E8A pod is supplied with the RSK product.

10.2. Mode Support

HEW connects to the Microcontroller and programs it via the E8A. Mode support is handled transparently to the user.

10.3. Breakpoint Support

HEW supports breakpoints on the user code, both in RAM and ROM.

Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

10.4. Memory Map

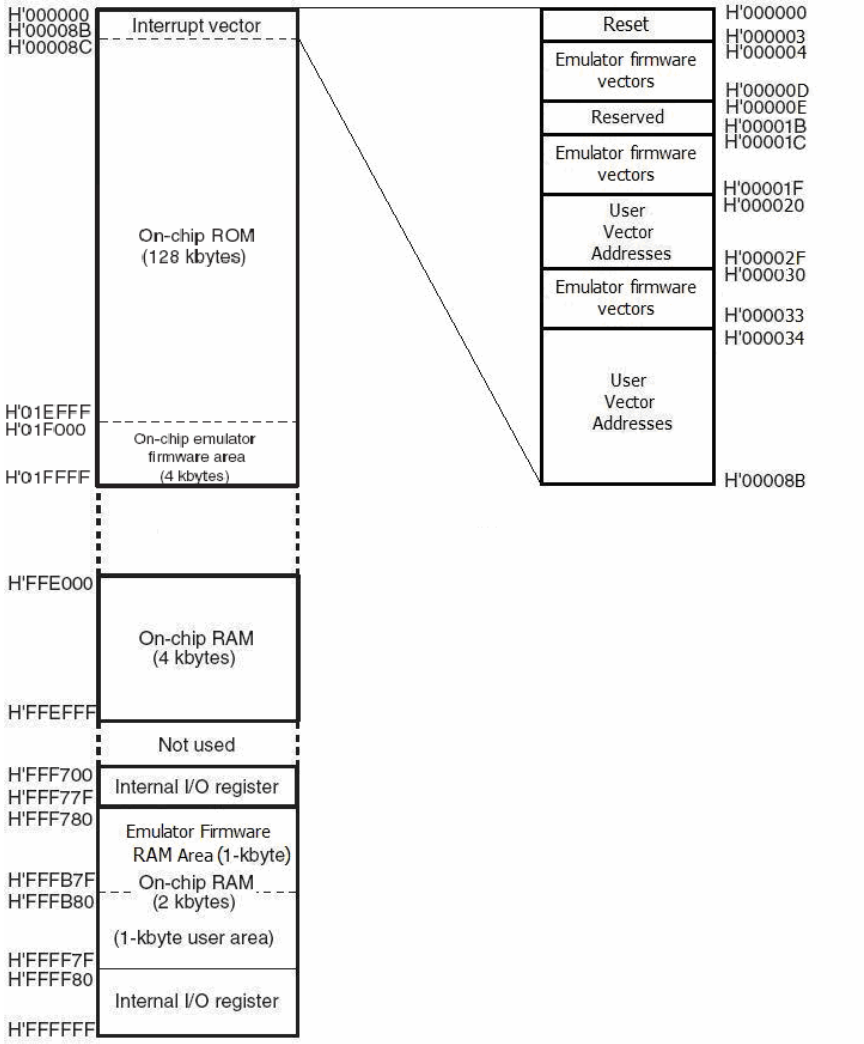

Figure 10-1: Memory Map

Chapter 11.Component Placement

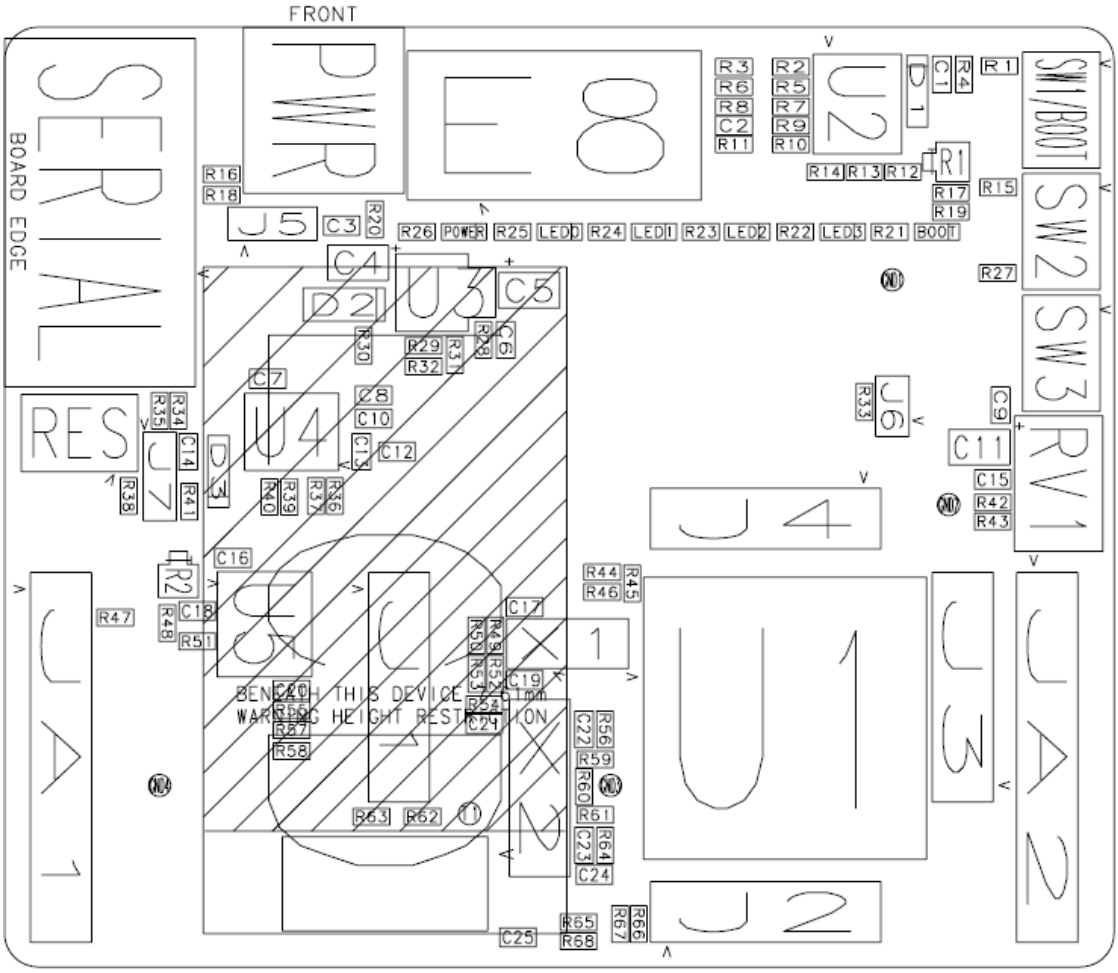

Figure 11-1: Component Placement

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW, refer to the HEW manual available on the CD or from the web site.

For information about the H8/36079 series microcontrollers refer to the H8/36079Group, H8/36077Group hardware manual.

For information about the H8/36079 assembly language, refer to the H8/300H Series Software Manual.

Online technical support and information is available at: http://www.renesas.com/renesas_starter_kits

Technical Contact Details

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Japan: csc@renesas.com

General information on Renesas Microcontrollers can be found on the Renesas website at: http://www.renesas.com/

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